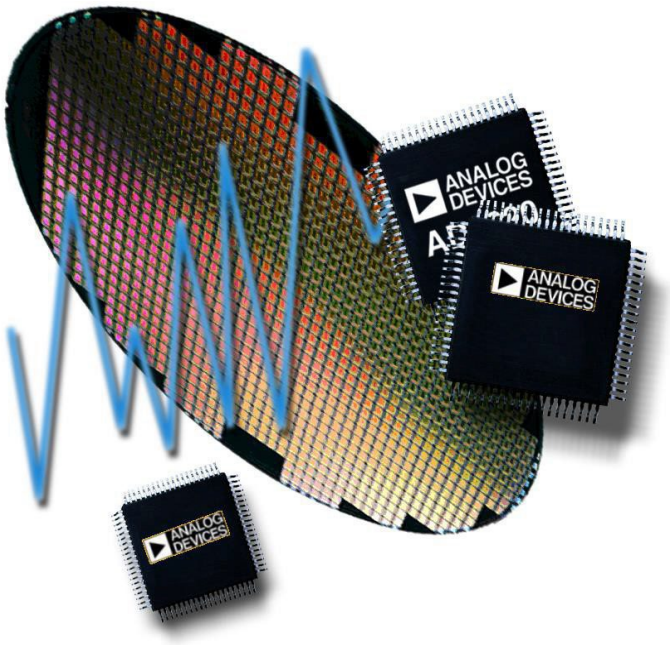

Reliability Report

Report Title: Analog Devices, Inc.
Beaverton Wafer Fab
0.18µm Process Qualification Report

Report Number: 25123

Revision: A

Date: 28 January 2026

N18 Process Overview

Reliability Results for the 0.18µm (N18) wafer fabrication processes at Analog Devices Beaverton, Oregon (ADBN) Wafer Fabrication Facility are summarized in this report.

To ensure maximum robustness and excellence in processing, the N18 processes are derived from 0.18µm technologies previously qualified at ADBN wafer fab.

In addition to sharing the same physical facility, environmental controls, process control plans and Quality Certifications, N18 employs identical design rules, and key process profiles, tools & materials as the legacy processes.

Process development featured unit level process outputs development, module integration, electrical WAT benchmarking and product yield and performance on identical sets of intrinsic devices and finished process.

Prior to release, Product performance of ADBN wafers is targeted against the baseline from the corresponding TSMC process.

Finally, selected Automotive and Consumer products from each process family are subjected to long loop reliability testing in accordance with industry standards JESD47 and AEC0Q100, as appropriate, as verification of process-to-product compatibility.

The following pages summarize those reliability results

Summary

ADBN N18 successfully passed reliability qualification tests. The process meets reliability standards required for release to manufacturing.

Based on >$2.3x10^6$ device-hours of high temperature Life Testing, the calculated failure rate for ADBN N18 is **0.5 FITS at 60% confidence level** when derated to 25˚C using activation energy of 0.7eV.

The FIT prediction is based on the following:

1. The 60% confidence level of failure rate is estimated using Chi square distribution.
2. Use Temperature assumed 25˚C
3. Arrhenius model is used with Ea=0.7eV
4. Thermal acceleration factor is (AFt) = exp[(Ea/kb) x (1/Tu – 1/Ts)]
5. FITs calculation: $\lambda = [\chi 2\ (\alpha, df) * 10^{\wedge}9] / [2 \times (\text{samples} \times 1\text{khrs} \times AFt]$

Qualification Vehicles

- AD8283 product is a 6-channel low noise preamplifier (LNA) with a programmable gain amplifier (PGA) and anti-aliasing filter (AAF) plus one direct-to-ADC channel, all integrated with a single 14-bit analog-to-digital converter (ADC), packaged in a 72 lead LFCSP. The AD8283 is qualified to AEC-Q100 Grade 2.

- ADV7392 product is 10-Bit SD/HD Video Encoder packaged in a 40 lead LFCSP and is qualified to AEC-Q100 Grade 2.

- ADDR9501 product is a complete satellite digital audio radio services (SDARS) RF front-end solution, providing a complete12.5 MHz SDARS frequency translation to a baseband signal using a single RF branch. The ADDR9501 is packaged in a 48 lead LFCSP and is qualified to AEC-Q100 Grade 2.

- MAX11390 product is a 24-bit, 6-channel, Delta-Sigma ADC packaged in a 6 x 6 bump array with 0.4mm bump pitch WLCSP package.

- ADV7391/ADV7392/ADV7393 product is an 8-bit/10-bit SD/HD Video Encoder packaged in a 40-lead LFCSP and qualified to AEC- Q100 Grade 2. The ADV7390/ADV7391/ADV7392/ADV7393 are a family of high-speed, digital-to-analog video encoders on single monolithic chips. Three 2.7 V/3.3 V, 10-bit video DACs (a single DAC for the WLCSP package) provide support for composite (CVBS), S-Video (Y-C), or component (YPrPb/RGB) analog outputs in either standard definition (SD) or high definition (HD) video formats.

- ADA8282 is a radar receive path AFE 4-Channel LNA and PGA. The LNA and PGA combine to form a signal chain that features a gain range of 18 dB to 36 dB in 6 dB increments with a guaranteed minimum bandwidth of 5 MHz.

- ADV7180 is a 10-Bit, 4× Oversampling SDTV Video Decoder. ADV7180 automatically detects and converts standard analog baseband television signals compatible with worldwide NTSC, PAL, and SECAM standards into 4:2:2 component video data compatible with the 8-bit ITU-R BT.656 interface standard.

- ADAR7251 is a 4-Channel, 16-Bit, Continuous Time Data Acquisition ADC designed especially for applications such as automotive LSR-FMCW or FSK-FMCW radar systems.

- ADE9000 is a highly accurate, fully integrated, multiphase energy and power quality monitoring device. Superior analog performance and a digital signal processing (DSP) core enable accurate energy monitoring over a wide dynamic range.

- AD2428W is an Automotive Audio Bus ($A^2B^®$) product which provides a multichannel, I^2S/TDM link over distances of up to 15 meters between nodes and is qualified to AEC-Q100 Grade 2.

- AD2433W is an Automotive Audio Bus ($A^2B^®$) product which provides a multichannel, I^2S/TDM link over distances of up to 15 meters between nodes and embeds bidirectional synchronous pulse-code modulation (PCM) data, clock, and synchronization signals onto a single unshielded twisted pair (UTP). AD2433 is qualified to AEC-Q100 Grade 2.

AECQ100 Qualification Test Methods and

AEC Test Group	AEC Stress Test Name	Abbreviation	AEC Test#	Reference
Group A ACCELERATED ENVIRONMENT STRESS TESTS	Preconditioning	PC	A1	By Part Number
	Temperature Humidity Bias or Biased-HAST	THB or HAST	A2	
	Autoclave or Unbiased HAST or Temperature Humidity (without Bias)	AC, UHST, or TH	A3	
	Temperature Cycle	TC	A4	
	Power Temperature Cycling	PTC	A5	
	High Temperature Storage Life	HTSL	A6	
Group B ACCELERATED LIFETIME SIMULATION TESTS	High Temperature Operating Life	HTOL	B1	By Part Number
	Early Life Failure Rate	ELFR	B2	
	NVM Endurance, Data Retention, and Operational Life	EDR	B3	
Group C PACKAGE ASSEMBLY INTEGRITY TESTS	Wire Bond Shear	WBS	C1	• Test C2 (and C1 for Cu Wire) • Tests C3-6 are qualified and controlled with inline monitors and may be viewed on-site at Analog Devices.
	Wire Bond Pull Strength	WBP	C2	
	Solderability	SD	C3	
	Physical Dimensions	PD	C4	
	Solder Ball Shear	SBS	C5	
	Lead Integrity	LI	C6	
Group D DIE FABRICATION RELIABILITY TESTS	Electromigration	EM	D1	Die Fabrication Reliability data may be viewed on-site at Analog Devices.
	Time Dependent Dielectric Breakdown	TDDB	D2	
	Hot Carrier Injection	HCI	D3	
	Negative Bias Temperature Instability	BTI	D4	
	Stress Migration	SM	D5	
Group E ELECTRICAL VERIFICATION TESTS	Pre- and Post-Stress Electrical Test	TEST	E1	By Part Number
	Electrostatic Discharge Human Body Model	HBM	E2	
	Electrostatic Discharge Charged Device Model	CDM	E3	
	Latch-Up	LU	E4	
	Electrical Distributions	ED	E5	• For Tests E5, E6 and E7, ADI New Product Yield Analysis Testing Guidelines meet AEC Q100 requirements. • Results for Tests E7-E11 are available as applicable on a case by case basis. • Test E12 results may be viewed on-site at Analog Devices
	Fault Grading	FG	E6	
	Characterization	CHAR	E7	
	Electromagnetic Compatibility	EMC	E9	
	Short Circuit Characterization	SC	E10	
	Soft Error Rate	SER	E11	
	Lead (Pb) Free	LF	E12	
Group F DEFECT SCREENING TESTS	Process Average Test	PAT	F1	ADI New Product Yield Analysis Testing Guidelines meet AECQ100Requirements.
	Statistical Bin/Yield Analysis	SBA	F2	
Group G CAVITYPACKAGE INTEGRITY TESTS	Mechanical Shock	MS	G1	< Applicable only for Cavity-Packages>
	Variable Frequency Vibration	VFV	G2	
	Constant Acceleration	CA	G3	
	Gross/Fine Leak	GFL	G4	
	Package Drop	DROP	G5	
	Lid Torque	LT	G6	
	Die Shear	DS	G7	
	Internal Water Vapor	IWV	G8	

AD8283, ADV7392, ADDR9501 Data

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.18µm CMOS at ADBN

Product Characteristics	Product(s) to be Qualified						
Generic/Root Part #	AD8283	AD8285	ADV7390	ADV7391	ADV7392	ADV7393	ADDR9501
Die Id	ND01	ND01	ND03	ND03	ND03	ND03	ND04
Die Size (mm)	7.00 x 7.00	7.00 x 7.00	2.57 x 3.05	2.57 x 3.05	2.57 x 3.05	2.57 x 3.05	3.67 x 4.54
Wafer Fabrication Site	ADBN	ADBN	ADBN	ADBN	ADBN	ADBN	ADBN
Wafer Fabrication Process	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Die Substrate	Si	Si	Si	Si	Si	Si	Si
Metallization / Layers	AlCu / 5	AlCu / 5	AlCu / 5	AlCu / 5	AlCu / 5	AlCu/5	AlCu / 6
Polyimide	Yes	Yes	No	No	No	No	Yes
Passivation	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results – 0.18μm CMOS at ADBN

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Early Life Failure Rate (ELFR)	B2	AEC Q100-008	T_a=125°C, T_j=134°C 48 Hours	AD8283	J90090.1	0/800	RH
					J91522.1	0/800	RH
					J91669.4	0/800	RH
			T_a=115°C, T_j=144°C 48 Hours	ADV7392	J93882.1	0/800	RH
					J95405.1	0/800	RH
High Temperature Operating Life (HTOL)	B1	JESD22-A108	T_a=125°C, T_j=134°C 1,000 Hours	AD8283	J90090.1	0/77	RCH
					J91522.1	0/77	RCH
					J93676.1	0/77	RCH
			T_a=115°C, T_j=144°C Biased, 1,000Hours	ADV7392	J93882.1	0/77	RCH
					J95405.1	0/77	RCH
					J91084.5	0/77	RCH
					J90861.1	0/77	RCH
					J90912.1	0/77	RCH
			T_a=100°C, T_j=134°C Biased, 1,000Hours	ADDR9501	J90227.3	0/77	RCH
					J90830.1	0/77	RCH
					J90914.1	0/77	RCH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 96 Hours	AD8283	J93676.1	0/76[2]	RH
					J91522.1	0/77	RH
					J91669.4	0/77	RH
			130°C, 85%RH 33.3 psia, Biased, 96 Hours	ADV7392	J91084.5	0/77	RH
					J90861.1	0/77	RH
					J90912.1	0/77	RH
			130°C, 85%RH 33.3 psia, Biased, 96 Hours	ADDR9501	J90227.3	0/77	RH
					J90830.1	0/77	RH
					J90914.1	0/77	RH

[1] These samples were subjected to preconditioning at MSL 3 with a 3x reflow peak temperature of 260°C before starting the stress test.
[2] Reduced sample size due to failures attributed to the electrically induced physical damage. See FA Report 274502.

Table 3: Package/Assembly Product Characteristics

Product Characteristics	Product(s) to be Qualified						
Generic/Root Part #	AD8283	AD8285	ADV7390	ADV7391	ADV7392	ADV7393	ADDR9501
Package	72-LFCSP	72-LFCSP	32-LFCSP	32-LFCSP	40-LFCSP	40-LFCSP	48-LFCSP
Body Size (mm)	10.00 x 10.00x 0.85	10.00 x 10.00x 0.85	5.00 x 5.00 x 0.75	5.00 x 5.00 x 0.75	6.00 x 6.00 x 0.75	6.00 x 6.00 x 0.75	7.00 x 7.00 x 0.85
Assembly Location	STATS (STA)	STATS (STA)	AMKOR (AP1)	ASE (AEK)	AMKOR (AP3)	AMKOR (AP1)	AMKOR (AP1)
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G700E	Sumitomo G700E	Sumitomo G700	Sumitomo G700	Sumitomo G700	Sumitomo G700	Sumitomo G700
Die Attach/Underfill/TIM	Ablestik 3230	Ablestik 3230	Ablestik 3230	Ablestik 3230	Ablestik 3230	Ablestik 3230	Ablestik 3230
Lead frame Material	Copper	Copper	Copper	Copper	Copper	Copper	Copper
Lead Finish	Sn	Sn	Sn	Sn	Sn	Sn	Sn
Wire Bond Material/Diameter (mils)	Gold / 1.00	Gold / 1.00	Gold / 1.00	Gold / 1.00	Gold / 1.00	Gold / 1.00	Gold / 1.00

Table 4: Package/Assembly Test Results

Test Name	AEC#	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Preconditioning	A1	J-STD-020	MSL-3	ADV7392	J87611.1	0/15	R
					J91084.5	0/15	R
					J90861.1	0/15	R
				AD8283	J87618.1	0/15	R
					J90090.1	0/15	R
					J91522.1	0/15	R
					J91669.4	0/15	R
				ADDR9501	J88476.1	0/15	R
					J90227.3	0/15	R
					J90830.1	0/15	R
					J90914.1	0/15	R
High Temperature Storage Life (HTSL)	A6	JESD22-A103	+150°C, 1,000 Hours	ADV7392	J87611.1	0/45	RH
					J91084.5	0/45	RH
				AD8283	J87618.1	0/45	RH
					J90090.1	0/45	RH
				ADDR9501	J88476.1	0/45	RH
					J90227.3	0/45	RH
Temperature Cycling (TC)[1]	A4	JESD22-A104	-55°C/+125°C, 1,000 Cycles	ADV7392	J87611.1	0/77	RH
					J91084.5	0/77	RH
					J90861.1	0/77	RH
					J90912.1	0/77	RH
				AD8283	J87618.1	0/77	RH
					J90090.1	0/77	RH
					J91522.1	0/77	RH
					J91669.4	0/77	RH
				ADDR9501	J88476.1	0/77	RH
					J90227.3	0/77	RH
					J90830.1	0/77	RH
					J90914.1	0/77	RH
Unbiased HAST (UHST)[1]	A3	JESD22-A118	+130°C, 85%RH 33.3 psia, 96 Hours	ADV7392	J87611.1	0/77	R
					J91084.5	0/77	R
					J90861.1	0/77	R
					J90912.1	0/77	R
				AD8283	J87618.1	0/77	R
					J90090.1	0/77	R
					J91522.1	0/77	R
					J91669.4	0/77	R
				ADDR9501	J88476.1	0/77	R
					J90227.3	0/77	R
					J90830.1	0/77	R
					J90914.1	0/77	R
Post-TCT WBP	C2	MIL-STD883 Method 2011	3gF	ADV7392	J87611.1	0/5	N/A
					J91084.5	0/5	N/A
				AD8283	J87618.1	0/5	N/A
					J90090.1	0/5	N/A
				ADDR9501	J88476.1	0/5	N/A
					J90227.3	0/5	N/A

[1] These samples were subjected to preconditioning at MSL 3 with a 3x reflow peak temperature of 260°C before starting the stress test.

ESD and Latch-Up Test Results

Table 5: ESD Test Results

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest
FICDM	ADV7392	40-LFCSP	JS-002	1Ω, Cpkg	±500V	C2	RH
	AD8283	72-LFCSP			±450V[1]	C1	RH
	ADDR9501	48-LFCSP			±750V	C2	RH
HBM	ADV7392	40-LFCSP	JS-001	1.5kΩ, 100pF	±2000V	1C	RH
	AD8283	72-LFCSP			±2000V	1C	RH
	ADDR9501	48-LFCSP			±2000V	1C	RH

[1] Control Material Passes SameThreshold

Table 6: Latch Up Test Results

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest
JESD78	ADV7392	+100mA, -100mA	+2.84V/+5.2V/+5.45V	+105°C	II	RH
	AD8283	+100mA, -100mA	+2.85V, +5.1V	125°C	II	RH
	ADDR9501	+100mA, -100mA	+2.85V, +5.1V	+85°C	II	RH

MAX11390 Data

Die/Fab Product Characteristics

Table 7: Die/Fab Product Characteristics- 0.18µm Mixed Mode CMOS at ADBN

Product Characteristics	Product(s) to be Qualified
Generic/Root Part #	MAX11390
Die Id	AZ33C
Die Size (mm)	2.84 x 2.84
Wafer Fabrication Site	ADBN
Wafer Fabrication Process	0.18µm Mixed Mode CMOS
Die Substrate	Si
Metallization / # Layers	AlCu / 5
Polyimide	No
Passivation	SiO_2/SiN

Die/Fab Test Results

Table 8: Die/Fab Test Results – 0.18μm Mixed Mode CMOS at ADBN

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Early Life Failure Rate (ELFR)[2]	AECQ100-008	Ta=125°C, P48	MAX11390	R44792A	0/1000
				R44792B	0/1000
				R44792C	0/1000
High Temperature Operating Life (HTOL) [2]	JESD22-A108	125°C<Tj<135°C, Biased, 1000 Hours, Ta=125°C	MAX11390	R44792A	0/77
				R44792B	0/76[3]
				R44792C	0/77
High Temperature Operating Life Corner Lots(CLHTOL) [2]	JESD22-A108	125°C‹Tj‹135°C, Biased, 1000 Hours	MAX11390	R44792C	0/154
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	110°C, 85%RH 33.3 psia, biased, 264 Hours	MAX11390	R44792A	0/77
				R44792B	0/77
				R44792C	0/77

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

[2] All Burn-in (HTOL & ELFR) was completed at Absolute Maximum Voltage (AMV = +3.6V; MOV =+3.3V).

[3] One (1) CMRR failure after 500 hours HTOL, likely damaged due to connection Issue between part to coupon/unit to socket during stress.

Table 9: Package/Assembly Product Characteristics

Product Characteristics	Product(s) to be Qualified
Generic/Root Part #	MAX11390
Package	36-Bump Thin WLP
Body Size (mm)	2.87 x 2.87 x 0.5
Assembly Location	ASE Kaohsiung, Taiwan
MSL/Peak Reflow Temperature(°C)	1 / 260°C
Bump Pitch (mm)	0.4
Bump Height (mm)	0.19
Bump Material	SAC125Ni

Table 10: Package/Assembly Test Results

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Preconditioning[1]	J-STD-020	MSL-1	MAX11390	R44792A	0/231
				R44792B	0/231
				R44792C	0/231
High Temperature Storage Life (HTSL)	JESD22-A103	+150°C, 1000 Hours	MAX11390	R44792A	0/77
				R44792B	0/77
				R44792C	0/77
Temperature Cycling (TC)[1]	JESD22-A104	-40°C/+125°C, 850 Cycles	MAX11390	R44792A	0/77
				R44792B	0/77
				R44792C	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	110°C, 85%RH 33.3 psia, biased, 264 Hours	MAX11390	R44792A	0/77
				R44792B	0/77
				R44792C	0/77
Unbiased HAST (UHST)[1]	JESD22-A118	+130°C, 85%RH 33.3 psia, 96 Hours	MAX11390	R44792A	0/77
				R44792B	0/77
				R44792C	0/77

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 11: ESD Test

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	MAX11390	36-Thin WLP	JS-002	1Ω, Cpkg	±1000V (All pins)	C3
HBM	MAX11390	36-Thin WLP	JS-001	1.5kΩ, 100pF	±3000V	2

Table 12: Latch Up Test

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class
JESD78	MAX11390	+250mA, -250mA	+3V/+5.4V	+85°C	II

Die/Fab Product Characteristics

Table 13: Die/Fab Product Characteristics- ADV7390/91/92/93 at ADBN

Product Characteristics	Product(s) to be Qualified			
Generic/Root Part #	ADV7390	ADV7391	ADV7392	ADV7393
Die Id	ND03	ND03	ND03	ND03
Die Size (mm)	2.57 x 3.05	2.57 x 3.05	2.57 x 3.05	2.57 x 3.05
Wafer Fabrication Site	ADBN	ADBN	ADBN	ADBN
Wafer Fabrication Process	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Die Substrate	Si	Si	Si	Si
Metallization / # Layers	AlCu / 5	AlCu / 5	AlCu / 5	AlCu/5
Polyimide	Yes	No	No	No
Passivation	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN

Die/Fab Test Results

Table 14: Die/Fab Test Results – ADV7390/91/92/93 at ADBN

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Early Life Failure Rate (ELFR)	B2	AEC Q100-008	T_A=115°C, T_J=144°C Biased, 48 Hours	ADV7392	J95405.1	0/800	RH
					J93882.1	0/800	RH
					J91084.5	0/800	RH
					J90861.1	0/800	RH
High Temperature Operating Life (HTOL)	B1	JESD22-A108	T_A=115°C, T_J=144°C Biased, 1,000 Hours	ADV7392	Q23099.1.HO1	0/77	RHC
					Q23099.2.HO2	0/77	RHC
					Q20017.1.HO1S	0/77	RHC
					Q20017.2.HO2S	0/77	RHC
					Q20017.3.HO3S	0/77	RHC
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130°C 85% RH 33.3 psia, Biased, 96 Hours	ADV7392	Q23099.1.HA1	0/77	RH
					Q23099.2.HA2	0/77	RH
					Q20017.1.HA1	0/77	RH
					Q20017.2.HA2	0/77	RH
					Q20017.3.HA3	0/77	RH

[1] These samples were subjected to preconditioning at MSL 1/3 with 3x reflow peak temp of 260°C before the start of the stress test.

ESD and Latch-Up Test Results

Table 15: ESD Test Results

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest
FICDM	ADV7392	40-LFCSP	JS-002	1Ω, Cpkg	±500V	C2	RH
HBM	ADV7392	40-LFCSP	JS-001	1.5kΩ, 100pF	±2000V	1C	RH

Table 16: Latch Up Test Results

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest
JESD78	ADV7392	+100mA, -100mA	+2.84V/+5.2V/+5.45V	+105°C	II	RH

ADA8282, ADV7180, ADAR7251 Data

Table 17: Die/Fab Product Characteristics- 0.18um Mixed Mode CMOS at ADBN

Product Characteristics	Product(s) to be qualified		
Generic/Root Part #	ADA8282	ADV7180	ADAR7251
Die Id	ND15A-0B A	ND17A-0A A	ND23A-0A A
Die Size (mm)	2.16 x 1.90	3.67 x 3.82	4.90 x 3.51
Wafer Fabrication Site	ADI Beaverton	ADI Beaverton	ADI Beaverton
Wafer Fabrication Process	0.18um Mixed Mode CMOS	0.18um Mixed Mode CMOS	0.18um Mixed Mode CMOS
Die Substrate	Si	Si	Si
Metallization / # Layers	AlCu(0.5%)/5	AlCu(0.5%)/5	AlCu(0.5%)/5
Polyimide	Yes	Yes	Yes
Passivation	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN

Die/Fab Test Results

Table 18: Die/Fab Test Results - 0.18um Mixed Mode CMOS at ADBN

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
ELF-AEC	B2	AEC Q100-008	Ta=125°C, Tj=127°C 48 hours	ADA8282	Q22785.1.EL1_RES_EXP	0/800	RH
					Q22785.2.EL2_RES_EXP	0/800	RH
					Q22785.3.EL3_RES_EXP	0/800	RH
			Ta= 125°C Tj=135°C 48 hours	ADV7180	Q23030.1.EL1_RES_EXP	0/800	RH
					Q23030.2.EL2_RES_EXP	0/800	RH
					Q23030.3.EL3_RES_EXP	0/800	RH
High Temperature Operating Life (HTOL)	B1	JESD22-A108	Ta=125°C, Tj=127°C 1000 hours	ADA8282	Q22785.1.HO1_RES_EXP	0/77	RCH
					Q22785.1.HO2_RES_EXP	0/77	RCH
					Q22785.2.HO3_RES_EXP	0/77	RCH
			Ta= 125°C Tj=135°C 1000 hours	ADV7180	Q23030.1.HO1_RES_EXP	0/77	RCH
					Q23030.2.HO2_RES_EXP	0/77	RCH
					Q23030.3.HO3_RES_EXP	1[2]/77	RCH
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 1,000 Hours	ADA8282	Q22785.1.HS1_RES_EXP	0/77	RH
				ADV7180	Q23030.1.HS1_RES_EXP	0/77	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADA8282	Q22785.1.HA1_RES_EXP	0/77	RH
					Q22785.2.HA2_RES_EXP	0/77	RH
					Q22785.3.HA3_RES_EXP	0/77	RH
				ADV7180	Q23030.1.HA1_RES_EXP	0/77	RH
					Q23030.2.HA2_RES_EXP	0/77	RH
					Q23030.3.HA3_RES_EXP	0/77	RH

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[2] One part failed electrical test following 500 hours HTOL. Refer to FA#282084.

Package/Assembly Product Characteristics

Table 19: Package/Assembly Product Characteristics - AMKOR Philippines

Product Characteristics	Product(s) to be qualified	
Generic/Root Part #	ADA8282	ADV7180
Package	32-LFCSP	40-LFCSP
Body Size (mm)	5.00 x 5.00 x 0.75	6.00 x 6.00 x 0.75
Assembly Location	AMKOR Philippines (AP3)	AMKOR Philippines (AP3)
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G700	Sumitomo G700
Die Attach/Underfill/TIM	Ablestik 3230 conductive	Ablestik 3230 conductive
Leadframe Material	Copper	Copper
Lead Finish	100Sn	100Sn
Wire Bond Material/Diameter (mils)	2N Gold / 1.00	2N Gold / 1.00

Package/Assembly Test Results

Table 20: Package/Assembly Test Results - LFCSP at AMKOR Philippines

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail /SS	eTest Temp
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 1,000 Hours	ADA8282	Q22785.1.HS1_RES_EXP	0/77	RH
				ADV7180	Q23030.1.HS1_RES_EXP	0/77	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADA8282	Q22785.1.HA1_RES_EXP	0/77	RH
					Q22785.2.HA2_RES_EXP	0/77	RH
					Q22785.3.HA3_RES_EXP	0/77	RH
				ADV7180	Q23030.1.HA1_RES_EXP	0/77	RH
					Q23030.2.HA2_RES_EXP	0/77	RH
					Q23030.3.HA3_RES_EXP	0/77	RH
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-3	ADA8282	Q22785.1.SH1_RES_EXP	0/11	R
					Q22785.2.SH2_RES_EXP	0/11	R
					Q22785.3.SH3_RES_EXP	0/11	R
				ADV7180	Q23030.1.SH1_RES_EXP	0/11	R
					Q23030.2.SH2_RES_EXP	0/11	R
					Q23030.3.SH3_RES_EXP	0/11	R
Temperature Cycling (TC)[1]	A4	JESD22-A104	-65°C/+150°C, 500 Cycles	ADA8282	Q22785.1.TC1_RES_EXP	0/77	RH
					Q22785.1.TC2_RES_EXP	0/77	RH
					Q22785.2.TC3_RES_EXP	0/77	RH
			-55°C/+150°C, 1000 Cycles	ADV7180	Q23030.1.TC1_RES_EXP	0/77	RH
					Q23030.2.TC2_RES_EXP	0/77	RH
					Q23030.3.TC3_RES_EXP	0/77	RH
Unbiased HAST (UHST)[1]	A3	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADA8282	Q22785.1.UH1_RES_EXP	0/77	R
					Q22785.1.UH2_RES_EXP	0/77	R
					Q22785.2.UH3_RES_EXP	0/77	R
				ADV7180	Q23030.1.UH1_RES_EXP	0/77	R
					Q23030.2.UH2_RES_EXP	0/77	R
					Q23030.3.UH3_RES_EXP	0/77	R
Wire Bond Pull	C2	MIL-STD-883, M2011	Post TCT, Single Duration	ADA8282	Q22785.1.WPPT1_RES_EXP	0/5	NA
				ADV7180	Q23030.1.WP1_RES_EXP_Au	0/5	NA

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 21: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest Temp
FICDM	ADA8282	32-LFCSP	AEC Q100-011	1Ω, Cpkg	±2000V	2	RH
	ADV7180	40-LFCSP			±750V	1B	RH
	ADAR7251	48-LFCSP_SS			±1000V	1C	RH
HBM	ADA8282	32-LFCSP	JS-001	1.5kΩ, 100pF	±4000V	3A	RH
	ADV7180	40-LFCSP			±4000V	3A	RH
	ADAR7251[1]	48-LFCSP_SS			±3000V	2	RH

[1]Supply pins tied together.

Table 22: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest Temp
JESD78	ADA8282	+150mA, -150mA	+5.4V	125°C	II	RH
	ADV7180	+100mA, -100mA	+5.4V	125°C	II	RH
	ADAR7251	+200mA, -200mA	+5.4V	125°C	II	RH

ADE9000 Data

Die/Fab Product Characteristics

Table 23: Die/Fab Product Characteristics- 0.18µm CMOS at ADBN

Product Characteristics	Product(s) to be Qualified	Products used for Substitution Data		
Generic/Root Part #	ADE9000	ADV7392	AD8283	ADDR9501
Die Id	ND20	ND03	ND01	ND04
Die Size (mm)	4.18 x 3.38	2.57 x 3.05	7.00 x 7.00	3.67 x 4.54
Wafer Fabrication Site	ADI Beaverton	ADI Beaverton	ADI Beaverton	ADI Beaverton
Wafer Fabrication Process	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Die Substrate	Si	Si	Si	Si
Metallization / Layers	AlCu / 5	AlCu / 5	AlCu / 5	AlCu / 6
Polyimide	No	No	Yes	Yes
Passivation	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN	SiO_2/SiN

Die/Fab Test Results

Table 24: Die/Fab Test Results – 0.18μm CMOS at ADBN

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Early Life Failure Rate (ELFR)	JESD74	T_a=125°C, T_j=134°C 48 Hours	AD8283	J90090.1	0/800
				J91522.1	0/800
				J91669.4	0/800
		T_a=115°C, T_j=144°C 48 Hours	ADV7392	J93882.1	0/800
				J95405.1	0/800
		T_a=125°C, T_j=131°C 48 Hours	ADE9000	J91955.1	0/800
				J95532.1	0/800
				K10341.1	0/800
High Temperature Operating Life (HTOL)[1]	JESD22-A108	T_a=125°C, T_j=134°C 1,000 Hours	AD8283	J90090.1	0/77
				J91522.1	0/77
				J93676.1	0/77
		T_a=115°C, T_j=144°C Biased, 1,000 Hours	ADV7392	J93882.1	0/77
				J95405.1	0/77
				J91084.5	0/77
				J90861.1	0/77
				J90912.1	0/77
		T_a=100°C, T_j=134°C Biased, 1,000 Hours	ADDR9501	J90227.3	0/77
				J90830.1	0/77
				J90914.1	0/77
		125°C<Tj<135°C, Biased, 1,000 Hours	ADE9000	J91955.1	0/77
				J95532.1	0/77
				K10341.1	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 96 Hours	AD8283	J93676.1	0/77
				J91522.1	0/77
				J91669.4	0/77
		130°C, 85%RH 33.3 psia, Biased, 96 Hours	ADV7392	J91084.5	0/77
				J90861.1	0/77
				J90912.1	0/77
		130°C, 85%RH 33.3 psia, Biased, 96 Hours	ADDR9501	J90227.3	0/77
				J90830.1	0/77
				J90914.1	0/77

[1] These samples were subjected to preconditioning at MSL 3 with a 3x reflow peak temperature of 260°C before starting the stress test.

Table 25: Package/Assembly Product Characteristics

Product Characteristics	Product(s) to be Qualified	Product(s) to be used as Substitution Data		
Generic/Root Part #	ADE9000	AD8283	ADV7392	ADDR9501
Package	40-LFCSP	72-LFCSP	40-LFCSP	48-LFCSP
Body Size (mm)	6.00 x 6.00 x 0.75	10.00 x 10.00 x 0.85	6.00 x 6.00 x 0.75	7.00x 7.00x 0.85
Assembly Location	ASE Korea	STATS (STA)	AMKOR (AP3)	AMKOR (AP1)
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G700LYT	Sumitomo G700E	Sumitomo G700	Sumitomo G700
Die Attach/Underfill/TIM	Hitachi EN 4900GC conductive	Ablestik 3230	Ablestik 3230	Ablestik 3230
Lead frame Material	Copper	Copper	Copper	Copper
Lead Finish	Sn	Sn	Sn	Sn
Wire Bond Material/Diameter (mils)	Gold / 1.00	Gold / 1.00	Gold / 1.00	Gold / 1.00

Table 26: Package/Assembly Test Results

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Preconditioning	J-STD-020	MSL-3	ADV7392	J91084.5	0/15
				J90861.1	0/15
				J90912.1	0/15
			AD8283	J90090.1	0/15
				J91522.1	0/15
				J91669.4	0/15
			ADDR9501	J90227.3	0/15
				J90830.1	0/15
				J90914.1	0/15
High Temperature Storage Life (HTSL)	JESD22- A103	+150°C, 1000 Hours	ADV7392	J91084.5	0/45
			AD8283	J90090.1	0/45
			ADDR9501	J90227.3	0/45
			ADE9000	J91955.1	0/45
				J95532.1	0/45
				K10341.1	0/45
Temperature Cycling (TC)[1]	JESD22- A104	-55°C/+125°C, 1000 Cycles	ADV7392	J91084.5	0/77
				J90861.1	0/77
				J90912.1	0/77
			AD8283	J90090.1	0/77
				J91522.1	0/77
				J91669.4	0/77
			ADDR9501	J90227.3	0/77
				J90830.1	0/77
				J90914.1	0/77
Unbiased HAST (UHST)[1]	JESD22- A118	+130°C, 85%RH 33.3 psia, 96 Hours	ADV7392	J91084.5	0/77
				J90861.1	0/77
				J90912.1	1/77
			AD8283	J90090.1	0/77
				J91522.1	0/77
				J91669.4	0/77
			ADDR9501	J90227.3	0/77
				J90830.1	0/77
				J90914.1	0/77
Post-TCT WBP	MIL-STD883 Method 2011	3gF	ADV7392	J91084.5	0/5
			AD8283	J90090.1	0/5
			ADDR9501	J90227.3	0/5

[1] These samples were subjected to preconditioning at MSL 3 with a 3x reflow peak temperature of 260°C before starting the stress test.

ESD and Latch-Up Test Results

Table 27: ESD Test Results

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	ADE9000	40-LFCSP	JESD22-C101	1Ω, Cpkg	±1250V	IV
HBM	ADE9000	40-LFCSP	JEDEC JS-001-2011 S-001	1.5kΩ, 100pF	±3750V	2

Table 28: Latch Up Test Results

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage
JESD78	ADE9000	+200mA, -200mA	+5.45V/+12.3V

AD2428W, A2433W Data

Die/Fab Product Characteristics

Table 29: Die/Fab Product Characteristics- 0.18µm BCDMOS

Product Characteristics	Product to be qualified	Qualification Vehicle
Generic/Root Part #	AD2433W	AD2428W
Die Id	NX20	ND02
Die Size (mm)	3.68 x 2.93	3.09 x 3.09
Wafer Fabrication Site	Analog Devices, Inc. Beaverton, OR	Analog Devices, Inc. Beaverton, OR
Wafer Fabrication Process	0.18µm BCDMOS	0.18µm BCDMOS
Die Substrate	Si	Si
Metallization / # Layers	AlCu(0.5%)/6	AlCu(0.5%)/6
Polyimide	Yes	Yes
Passivation	undoped-oxide/SiN	undoped-oxide/SiN

Die/Fab Test Results

Table 30: Die/Fab Test Results - 0.18µm BCDMOS at Analog Devices - Beaverton

Test Name	AEC #	Spec	Conditions	Generic/ Root Part #	Lot #	Fail/SS	eTest Temp
Early Life Failure Rate (ELFR)	B2	AEC Q100-008	T_A = 105°C, T_J = 125°C, 48 Hours	AD2428W	Q20034.1.15A	0/200	RH
					Q20034.1.15B	0/200	RH
					Q20034.1.15C	0/200	RH
					Q20034.1.15D	0/200	RH
					Q20034.2.6A	0/200	RH
					Q20034.2.6B	0/200	RH
					Q20034.2.6C	0/200	RH
					Q20034.2.6D	0/200	RH
			T_A = 125°C, 48Hours		Q20034.1.1A	0/217	RH
					Q20034.1.1B	0/216	RH
					Q20034.1.1C	0/216	RH
					Q20034.1.1D	0/151	RH
High Temperature Operating Life (HTOL)	B1	JESD22-A108	TA = 105°C, TJ = 125°C, 2,000 Hours	AD2428W	Q20034.1.10	0/77	RHC
					Q20034.2.1	0/77	RHC
					Q20034.1.1	0/77	RHC
High Temperature Operating Life (HTOL)[1]			T_A = 105°C, T_J = 125°C, 1,000 Hours	AD2433W	Q22565.1.1	0/77	RHC
High Temperature Operating Life (HTOL)							
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 1,000Hours	AD2428W	Q20034.1.2	0/45	RH
Highly Accelerated Stressed Test(HAST)[1]	A2	JESD22-A110	130°C, 85%RH, 33.3 psia, Biased, 96 Hours	AD2428W	Q20034.1.6	0/77	RH
					Q20034.1.11	0/77	RH
					Q20034.2.2	0/77	RH
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-3	AD2433W	Q22565.1.4	0/11	R
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 500Hours		Q22565.1.3	0/45	RH
Highly Accelerated Stressed Test(HAST)[1]	A2	JESD22-A110	130°C, 85%RH, 33.3 psia, Biased, 96 Hours		Q22565.1.2	0/77	RH
Unbiased HAST (UHST)[1]	A3	JESD22-A118	130°C, 85%RH, 33.3 psia, Unbiased, 96 Hours		Q22565.1.6	0/77	RH

1. These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Package/Assembly Product Characteristics

Table 31: Package/Assembly Product Characteristics - 48-LFCSP at STATS (SC3)

Product Characteristics	Product(s) to be qualified	
Generic/Root Part #	AD2433W	AD2428W
Package	48-LFCSP_SS	32-LFCSP_SS
Body Size (mm)	7.00 x 7.00 x 0.75	5.00 x 5.00 x 0.75
Assembly Location	STATS (SC3)	UTAC (UT2)
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G700LA	Sumitomo G700LTD
Die Attach/Underfill/TIM	Hitachi EN 4900GC Conductive	Ablestik 8600 Conductive
Leadframe Material	Copper	Copper
Lead Finish	Matte Sn	Matte Sn
Wire Bond Material/Diameter (mils)	PdCuAu 3N / 0.80	GMG 4N Gold / 1.00

Package/Assembly Test Results

Table 32 Package/Assembly Test Results – LFCSP_SS at STATS (SC3) and UTAC (UT2)

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 1,000 Hours	AD2428W	Q20034.1.2	0/45	RH
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-3	AD2428W	Q20034.1.14	0/11	R
					Q20034.1.3	0/11	R
					Q20034.2.5	0/11	R
Temperature Cycling (TC)[1]	A4	JESD22-A104	-65°C/+150°C, 1,000 Cycles	AD2428W	Q20034.1.4	0/77	RH
					Q20034.1.12	0/77	RH
					Q20034.2.3	0/77	RH
Unbiased HAST (UHST)[1]	A3	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD2428W	Q20034.1.13	0/77	R
					Q20034.1.5	0/77	R
					Q20034.2.4	0/77	R
Highly Accelerated Stressed Test(HAST)[1]	A2	JESD22-A110	130°C, 85%RH, 33.3 psia, Biased, 96 Hours	AD2428W	Q20034.1.6	0/77	RH
					Q20034.1.11	0/77	RH
					Q20034.2.2	0/77	RH
Wire Bond Pull	A4	MIL-STD-883, M2011	Post-TCT	AD2428W	Q20034.1.15	0/5	-
					Q20034.2.6	0/5	-
					Q20034.3.1	0/5	-
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-3	AD2433W	Q22565.1.4	0/11	R
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 500 Hours		Q22565.1.3	0/45	RH
Highly Accelerated Stressed Test (HAST)[1]	A2	JESD22-A110	130°C, 85%RH, 33.3 psia, Biased, 96 Hours		Q22565.1.2	0/77	RH
Unbiased HAST (UHST)[1]	A3	JESD22-A118	MSL130°C, 85%RH, 33.3 psia, Biased, 96 Hours		Q22565.1.6	0/77	RH

1. These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 33: ESD Test

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest Temp
FICDM	AD2433W	48-LFCSP_SS	AEC Q100-011	1Ω, Cpkg	±1250V	C3	RH
	AD2428W	32-LFCSP_SS			±1250V		
HBM	AD2428W	32-LFCSP_SS	AEC-Q100-002	1.5kΩ, 100pF	±2000V	2	RH
	AD2433W	48-LFCSP_SS			±2000V	2	RH

Table 34: Latch Up Test

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest Temp
JESD78	AD2428W	+200mA, -200mA	+2.97/5.445/12.0V	105°C	II	RH
JESD78	AD24433W	+200mA, -200mA	+2.97/5.445/12.0V	105°C	II	RH